Exhibit 12

Paper No. 13

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner

IPR2022-00639
Patent No. 10,949,339

PETITIONER'S AUTHORIZED
REPLY TO PATENT OWNER'S PRELIMINARY RESPONSE

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CLAIM LISTING

Ref. #	Listing of Challenged Claims
[1pre]	A N-bit-wide memory module mountable in a memory socket of a computer system and configurable to communicate with a memory controller of the computer system via address and control signal lines and N-bit wide data signal lines, the N-bit wide data signal lines including a plurality of sets of data signal lines, each set of data signal lines is a byte wide, the memory module comprising:
[1a]	a printed circuit board (PCB) having an edge connector comprising a plurality of electrical contacts which are positioned on an edge of the PCB and configured to be releasably coupled to corresponding contacts of the memory socket;
[1b]	double data rate dynamic random access memory (DDR DRAM) devices coupled to the PCB and arranged in multiple N-bit-wide ranks;
[1c1]	a module controller coupled to the PCB and operatively coupled to the DDR DRAM devices, wherein the module controller is configurable to receive from the memory controller via the address and control signal lines input address and control signals for a memory write operation to write N-bit-wide write data from the memory controller into a first N-bit-wide rank of the multiple N-bit-wide ranks, and to output registered address and control signals in response to receiving the input address and control signals,
[1c2]	wherein the registered address and control signals cause the first N-bit-wide rank to perform the memory write operation by receiving the N-bit-wide write data, wherein the module controller is further configurable to output module control signals in response to at least some of the input address and control signals; and
[1d1]	a plurality of byte-wise buffers coupled to the PCB and configured to receive the module control signals

Ref. #	Listing of Challenged Claims
[1d2]	wherein each respective byte-wise buffer of the plurality of byte-wise buffers has a first side configured to be operatively coupled to a respective set of data signal lines, a second side that is operatively coupled to at least one respective DDR DRAM device in each of the multiple N-bit-wide ranks via respective module data lines, and a byte-wise data path between the first side and the second side,
[1d3]	wherein the each respective byte-wise buffer is disposed on the PCB at a respective position corresponding to the respective set of the plurality of sets of data signal lines;
[1e]	wherein the each respective byte-wise buffer further includes logic configurable to control the byte-wise data path in response to the module control signals, wherein the byte-wise data path is enabled for a first time period in accordance with a latency parameter to actively drive a respective byte-wise section of the N-bit wide write data associated with the memory operation from the first side to the second side during the first time period; and
[1f]	wherein the byte-wise data path includes first tristate buffers, and the logic in response to the module control signals is configured to enable the first tristate buffers to drive the respective byte-wise section of the N-bit wide write data to the respective module data lines during the first time period.
[2a]	The memory module of claim 1, wherein the DDR DRAM devices each has a bit width of 4 bits, wherein the at least one respective DDR DRAM device in each of the multiple N-bit-wide ranks includes a respective pair of DDR DRAM devices,
[2b]	wherein a first subset of the first tristate buffers is enabled for the first time period to drive a first nibble of the respective byte-wise section of the N-bit wide write data to a first subset of the respective module data lines coupled to a first one of the respective pair of DDR DRAM devices in each of at least some of the multiple N-bit-wide ranks,

Ref. #	Listing of Challenged Claims
[2c]	while a second subset of the first tristate buffers is enabled for the first time period to drive a second nibble of the respective byte-wise section of the N-bit wide write data to a second subset of the respective module data lines coupled to a second one of the respective pair of DDR DRAM devices in each of at least some of the multiple N-bit-wide ranks.
[3a]	The memory module of claim 2, wherein the byte-wise data path further includes a set of write buffers configurable to receive the respective byte-wise section of the N-bit wide write data from the respective set of data signal lines ...
[3b]	... before the first tristate buffers regenerate and drive the respective byte-wise section of the N-bit wide data to the second side of the each respective byte-wise buffer.
[4]	The memory module of claim 3, wherein each of the write buffers is comparable to an input buffer on one of the DDR DRAM devices such that the each respective byte-wise buffer presents to the memory controller one DDR DRAM device load during the memory operation.
[5]	The memory module of claim 1, wherein the DDR DRAM devices each has a bit width of 8 bits, and wherein the at least one respective DDR DRAM device in each of the multiple N-bit-wide ranks includes a single DDR DRAM device.
[6]	The memory module of claim 1, wherein the logic is configurable to enable the first tristate buffers at a beginning of the first time period and to disable the first tristate buffers at an end of first time period.
[7]	The memory module of claim 1, wherein the module controller is configured to use the module control signals to control timing of the first time period in accordance with the latency parameter.

Ref. #	Listing of Challenged Claims
[8]	The memory module of claim 1, wherein the registered address and control signals include rank select signals, the rank select signals including one rank select signal for each of the multiple N-bit-wide ranks, and wherein the rank select signal received by the first N-bit-wide rank is different from the rank select signal received by any other N-bit-wide rank of the multiple N-bit-wide ranks.
[9]	The memory module of claim 8, wherein each of the respective module data lines is configured to carry data from the memory controller to a corresponding memory device in each of the multiple N-bit-wide ranks during the memory write operation.

Ref. #	Listing of Challenged Claims
[10]	The memory module of claim 1, wherein: the module controller is further configurable to receive from the memory controller via the address and control signal lines additional input address and control signals for a memory read operation to read N-bit-wide read data from the memory controller from a second N-bit-wide rank of the multiple N-bit-wide ranks, and to output additional registered address and control signals in response to the additional input address and control signals; the second N bit-wide rank is configurable to output the N bit-wide read data associated with the memory read operation in response to at least some of the additional registered address and control signals; the module controller is further configurable to output additional module control signals in response to the additional input address and control signals; the logic in the each respective byte-wise buffer is further configurable to control the byte-wise data path in response to the additional module control signals, wherein the byte-wise data path is enabled for a second time period to actively drive a respective byte-wise section of the N bit wide read data associated with the memory read operation from the second side to the first side during the second time period in response to the additional module control signals; the byte-wise data path further includes second tristate buffers configurable to be enabled by the logic to drive the respective byte-wise section of the N-bit wide read data to the respective set of data signal lines during the second time period; and the second tristate buffers are disabled during the first time period and the first tristate buffers are disabled during the second time period.
[11pre]	A N-bit-wide memory module mountable in a memory socket of a computer system and configured to communicate with a memory controller of the computer system via address and control signal lines and N-bit wide data signal lines, the N-bit wide data signal lines including a plurality of sets of data signal lines, the memory module comprising:

Ref. #	Listing of Challenged Claims
[11a]	a printed circuit board (PCB) having an edge connector comprising a plurality of electrical contacts which are positioned on an edge of the PCB and are configured to be releasably coupled to corresponding contacts of the memory socket;
[11b]	double data rate dynamic random access memory (DDR DRAM) devices coupled to the PCB and arranged in multiple N-bit-wide ranks, each N-bit-wide rank includes n DDR DRAM devices;
[11c1]	n/2 data transmission circuits mounted on the PCB,
[11c2]	wherein each of the n/2 data transmission circuits is disposed on the PCB at respective positions corresponding to a respective set of data signal lines among the plurality of sets of data signal lines, and
[11c3]	wherein the each of the n/2 data transmission circuits has a first side configured to be operatively coupled to the respective set of data signal lines, a second side that is operatively coupled to a respective pair of DDR DRAM devices in each of the multiple ranks via respective module data lines, and data paths between the first side and the second side;
[11d1]	a module controller coupled to the PCB and operatively coupled to the DDR DRAM devices, the module controller being configurable to receive from the memory controller via the address and control signal lines input address and control signals for a memory write operation to write N-bit-wide write data from the memory controller into a first N-bit-wide rank among the multiple N-bit-wide ranks, and to output registered address and control signals in response to the input address and control signal,
[11d2]	wherein the registered address and control signals cause the first N-bit-wide rank to perform the memory write operation by receiving the N-bit-wide write data, wherein the module controller is further configurable to transmit module control signals to the n/2 data transmission circuits in response to the input address and control signals; and

Ref. #	Listing of Challenged Claims
[11e1]	wherein, in response to the module control signals, each respective data transmission circuit is configurable to enable the data paths for a first time period in accordance with a latency parameter to actively drive a respective section of the N-bit wide write data associated with the memory operation from the first side to the second side during the first time period,
[11e2]	wherein a first subsection of the respective section of the N-bit wide write data output from the second side of the each respective data transmission circuit is written into a first one of the respective pair of DDR DRAM devices in the first N-bit wide rank, while a second subsection of the respective section of the N-bit wide write data output from the second side of the each respective data transmission circuit is written into a second one of the respective pair of DDR DRAM devices in the first N-bit wide rank; and
[11f1]	wherein the data paths includes first tristate buffers, and the respective data transmission circuit in response to the module control signals is configured to enable a first subset of the first tristate buffers to drive the first subsection of the respective section of the N-bit wide write data to a first subset of the respective module data lines coupled to a first one of the respective pair of DDR DRAM devices in each of at least some of the multiple N-bit-wide ranks, and ...
[11f2]	... to enable a second subset of the first tristate buffers to drive a second subsection of the respective section of the N-bit wide write data to a second subset of the respective module data lines coupled to a second one of the respective pair of DDR DRAM devices in each of at least some of the multiple N-bit-wide ranks.
[12]	The memory module of claim 11, wherein the registered address and control signals include a rank select signal for each of the multiple N-bit wide ranks, the rank select signal for the first N-bit wide rank is different from the rank select signal for any other N-bit wide rank of the multiple N-bit wide ranks.

Ref. #	Listing of Challenged Claims
[13]	The memory module of claim 12, wherein each of the respective module data lines is configured to carry data from the memory controller to a corresponding memory device in each of the multiple N-bit-wide ranks during the memory operation.
[14a]	The memory module of claim 13, wherein the data paths further include a set of write buffers configurable to receive the respective section of the N-bit wide data from the respective set of data signal lines ...
[14b]	... before the respective section of the N-bit wide write data is regenerated and driven by—the first tristate buffers to the respective module data lines.
[15]	The memory module of claim 14, wherein each of the set of write buffers is comparable in loading to an input buffer on one of the DDR DRAM devices such that the each respective data transmission circuit presents to the memory controller one DDR DRAM device load during the memory write operation.
[16]	The memory module of claim 11, wherein the module controller is configurable to use the module control signals to control timing of the first time period in accordance with the latency parameter.
[17]	The memory module of claim 11, wherein the each respective data transmission circuit is configured to present to the memory controller one DDR DRAM device load on each of the respective set of data lines during the memory write operation.

Ref. #	Listing of Challenged Claims
[18]	The memory module of claim 11, wherein: the module controller is further configurable to receive from the memory controller via the address and control signal lines additional input address and control signals for a subsequent memory read operation to read N bit-wick: read data from a second N-bit-wide rank of the multiple N-bit-wide ranks, and to output additional registered address and control signals in response to the additional input address and control signals; the second N-bit-wide rank of the multiple N-bit-wide ranks is configurable to output the N-bit-wide read data associated with the memory read operation in response to at least some of the additional registered address and control signals; the module controller is further configurable to output additional module control signals in response to the additional input address and control signals; and the each respective data transmission circuit is further configurable to enable the data paths for a second time period to actively drive a respective section of the N-bit wide read data associated with the memory read operation from the second side to the first side during the second time period in response to the additional module control signals; the data paths further includes second tristate buffers configurable to be enabled during the second time period to drive the respective section of the N-bit wide read data to the respective set of data signal lines; and the each respective data transmission circuit is further configurable to keep the second tristate buffers disabled during the first time period and to keep the first tristate buffers disabled during the second time period.
[19pre]	A N-bit-wide memory module mountable in a memory socket of a computer system and configured to communicate with a memory controller of the computer system via address and control signal lines and N-bit wide data signal lines, the N-bit wide data signal lines including a plurality of sets of data signal lines, the memory module comprising:

Ref. #	Listing of Challenged Claims
[19a]	a printed circuit board (PCB) having an edge connector comprising a plurality of electrical contacts which are positioned on an edge of the PCB and are configured to be releasably coupled to corresponding contacts of the memory socket;
[19b]	double data rate dynamic random access memory (DDR DRAM) devices coupled to the PCB arranged in multiple N-bit-wide ranks;
[19c1]	a module controller coupled to the PCB and operatively coupled to the DDR DRAM devices, the module controller being configurable to receive from the memory controller via the address and control signal lines first address and control signals for a first memory operation to read first N-bit-wide data from a first N-bit-wide rank among the multiple ranks and to subsequently receive second address and control signals for a second memory operation to read second N-bit-wide data from a second N-bit-wide rank among the multiple ranks,
[19c2]	the module controller being further configurable to output first registered address and control signals for the first memory operation in response to receiving the first address and control signals and to output second registered address and control signals for the second memory operation in response to receiving the second address and control signals,
[19c3]	wherein the first registered address and control signals cause the first N-bit-wide rank to output the first N-bit-wide data associated with the first memory operation, and the second registered address and control signals cause the second N-bit-wide rank to output the second N-bit-wide data associated with the second memory operation,
[19c4]	wherein the module controller is further configurable to output first module control signals for the first memory operation in response to receiving the first address and control signals and to output second module control signals for the second memory operation in response to receiving the second address and control signals; and

Ref. #	Listing of Challenged Claims
[19d1]	a plurality of buffers coupled to the PCB and configured to receive the first module control signals and to receive the second module control signals,
[19d2]	wherein each respective buffer of the plurality of buffers has a first side that is operatively coupled to a respective set of data signal lines, a second side that is operatively coupled to at least one respective DDR DRAM device in each of the multiple N-bit-wide ranks via respective module data lines, and data paths between the first side and the second-side,
[19d3]	wherein the each respective buffer is disposed on the PCB at a respective position corresponding to the respective set of the plurality of sets of data signal lines;
[19e1]	wherein the each respective buffer further includes logic configurable to enable the data paths for a first time period to actively drive a respective section of the first N-bit wide data associated with the first memory operation from the second side to the first side during the first time period, and to enable the data paths for a second time period subsequent to the first time period to actively drive a respective section of the second N-bit wide data associated with the second memory operation from the second side to the first side during the second time period,
[19e2]	wherein the data paths are disabled after the first time period and before the second time period.
[20a]	The memory module of claim 19, wherein the DDR DRAM devices each has a bit width of 4 bits,
[20b]	wherein the at least one respective DDR DRAM device in each of the multiple N-bit-wide ranks includes a respective pair of DDR DRAM devices, and
[20c]	wherein a first nibble of the respective section of the first N bit wide data is output by a first one of the respective pair of DDR DRAM devices in the first N-bit wide rank ...

Ref. #	Listing of Challenged Claims
[20d]	... while a second nibble of the respective section of the first N bit wide data is output by a second one of the respective pair of DDR DRAM devices in the first N-bit wide rank.
[21]	The memory module of claim 19, wherein the module controller is configured to use the first module control signals to control timing of the first time period in accordance with a latency parameter and to use the second module control signals to control timing of the second time period in accordance with the latency parameter.
[22]	The memory module of claim 19, wherein the each respective buffer is configured to present to the at least one respective DDR DRAM device a load that is similar to that of the memory controller during the first or the second memory operation.
[23]	The memory module of claim 19, wherein the first registered address and control signals include a first set of rank select signals corresponding to respective ones of the multiple N-bit wide ranks, the first set of rank select signals including a first rank select signal received by the first N-bit wide rank that is different from each of the other rank select signals in the first set of rank select signals, and wherein the second registered address and control signals include a second set of rank select signals corresponding to respective ones of the multiple N-bit wide ranks, the second set of rank select signals including a second rank select signal received by the second N-bit wide rank that is different from each of the other rank select signals in the second set of rank select signals.
[24]	The memory module of claim 23, wherein each of the respective module data lines is configured to carry data from the memory controller to a corresponding memory device in each of the multiple N-bit-wide ranks.
[25a]	The memory module of claim 19, wherein the data path includes at least a first input buffer and ...
[25b]	... a second buffer for each bit of the respective section of the first or second N-bit wide data,

Ref. #	Listing of Challenged Claims
[25c]	wherein the first buffer is configured to receive the each bit from the second side of the each respective buffer, and ...
[25d]	... the second buffer is configured to regenerate and drive the each bit to the first side of the each respective buffer,
[25e]	wherein at least the second buffer is a tristate buffer configurable to be enabled by the logic in response to the first or second module control signals, and
[25f]	wherein the first [sic] buffer is comparable to an output buffer on one of the DDR DRAM devices.
[26a]	The memory module of claim 19, wherein the data paths include a set of input buffers configurable to receive the respective section of the first or second N-bit wide data from the respective set of module data lines and ...
[26b]	... a set of output buffers configurable to regenerate and drive the respective section of the first or second N-bit wide data to the first side,
[26c]	wherein at least the set of output buffers are tristate buffers configurable to be enabled by the logic during the first time period in response to the first module control signals and during the second time period in response to the second module control signals, and
[26d]	wherein at least the set of output buffers are disabled by the logic after the first time period and before the second time period.
[27pre]	A memory module mountable in a memory socket of a computer system and configurable to communicate with a memory controller of the computer system via address and control signal lines and data signal lines, the data signal lines including a plurality of sets of data signal lines, each set of data signal lines is n bit wide, the memory module comprising:

Ref. #	Listing of Challenged Claims
[27a]	a printed circuit board (PCB) having an edge connector comprising a plurality of electrical contacts which are positioned on an edge of the PCB and are configured to be releasably coupled to corresponding contacts of the memory socket;
[27b1]	a module controller coupled to the PCB and configurable to receive from the memory controller via the address and control signal lines first address and control signals for a memory write operation and to subsequently receive second address and control signals for a memory read operation,
[27b2]	the module controller being further configurable to output first registered address and control signals and first module control signals for the memory write operation in response to the first address and control signals, and to output second registered address and control signals and second module control signals for the memory read operation in response to the second address and control signals; and
[27c1]	double data rate dynamic random access memory (DDR DRAM) devices coupled to the PCB and ...
[27c2]	... configurable to perform the memory write operation by receiving write data in response to the first registered address and control signals, and to perform the memory read operation by outputting read data in response to the second registered address and control signals; and
[27d1]	a plurality of n-bit-wide data buffers coupled to the PCB and configured to receive the first module control signals and subsequently the second module control signals,
[27d2]	wherein each respective n-bit-wide data buffer of the plurality of n-bit-wide data buffers has a first side that is operatively coupled to a respective set of data signal lines, and a second side that is operatively coupled to a respective n-bit-wide section of the DDR DRAM devices via respective module data lines, wherein:

Ref. #	Listing of Challenged Claims
[27d3a]	the each respective n-bit-wide data buffer includes a first set of input buffers configurable to receive a respective n-bit section of the write data from the respective set of data signal lines,
[27d3b]	a first set of tristate buffers configurable to drive the respective n-bit section of the write data to the respective module data lines,
[27d3c]	a second set of input buffers configurable to receive a respective n-bit section of the read data from the respective module data lines,
[27d3d]	a second set of tristate buffers configurable to drive the respective n-bit section of the read data to the respective set of data signal lines, and
[27d3e]	logic configurable to control at least the first set of tristate buffers and the second set of tristate buffers;
[27d4]	the logic in response to the first module control signals is configured to enable the first set of tristate buffers for a first time period corresponding to the memory write operation to drive the respective n-bit section of the write data;
[27d5]	the logic in response to the second module control signals is configured to enable the second set of tristate buffers for a second time period corresponding to the memory read operation to drive the respective n-bit section of the read data;
[27d6]	the first set of tristate buffers are disabled during the second time period; and
[27d7]	the second set of tristate buffers are disabled during the first time period.

Ref. #	Listing of Challenged Claims
[28]	The memory module of claim 27, wherein the logic is configurable to keep the first set of tristate buffers and the second set of tristate buffers disabled when the memory module is not targeted by the memory controller for any memory operations.
[29a]	The memory module of claim 27, wherein: the DDR DRAM devices include a plurality of ranks of DDR DRAM devices;
[29b]	the each respective n-bit-wide buffer is coupled to at least one respective DDR DRAM device in each of the plurality of ranks via the respective module data lines;
[29c]	the first registered address and control signals cause one rank of DDR DRAM devices to perform the memory write operation by receiving the write data; and
[29d]	the second registered address and control signals cause one rank of DDR DRAM devices to perform the memory read operation by outputting the read data.
[30a]	The memory module of claim 29, wherein: the at least one respective DDR DRAM device in each of the plurality of ranks includes a respective pair of DDR DRAM devices;
[30b]	a first n/2-bit section of the respective n-bit section of the write_data is driven by a first subset of the first set of tristate buffers to a first one of the respective pair of DDR DRAM devices in the one rank of DDR DRAM devices performing the memory write operation;
[30c]	a second n/2-bit section of the respective n-bit section of the write_data is driven by a second subset of the first set of tristate buffers to a second one of the respective pair of DDR DRAM devices in the one rank of DDR DRAM devices performing the memory write operation;

Ref. #	Listing of Challenged Claims
[30d]	a first n/2-bit section of the respective n-bit section of the read_data is received by a first subset of the second set of input buffers from a first one of the respective pair of DDR DRAM devices in the one rank of DDR DRAM devices performing the memory read operation; and
[30e]	a second n/2-bit section of the respective n-bit section of the read_data is received by a second subset of the second set of input buffers from the second one of the respective pair of DDR DRAM devices in the one rank of DDR DRAM devices performing the memory read operation.
[31a]	The memory module of claim 29, wherein: the at least one respective DDR DRAM device in each of the plurality of ranks includes one respective DDR DRAM;
[31b]	the respective n-bit section of the write_data is driven by the first set of tristate buffers to the respective DDR DRAM device in the one rank of DDR DRAM devices performing the memory write operation; and
[31c]	the respective n-bit section of the read_data is received by the second set of input buffers from the respective DDR DRAM device in the one rank of DDR DRAM devices performing the memory read operation.
[32]	The memory module of claim 29, wherein each of the respective module data lines is configured to carry data from the memory controller to a corresponding memory device in each of the plurality of ranks.

<table>
<tr><th>Ref. #</th><th>Listing of Challenged Claims</th></tr>
<tr><td>[33]</td><td>The memory module of claim 29, wherein:

the module controller is further configurable to receive from the memory controller via the address and control signal lines third address and control signals for a subsequent memory read operation, and to output third registered address and control signals and third module control signals for the subsequent memory read operation in response to receiving the third address and control signals;

the DDR DRAM devices are configurable to perform the subsequent memory read operation by outputting additional read data in response to the third registered address and control signals;

the subsequent memory read operation is performed by another rank of DDR DRAM devices that is different from the one rank of DDR DRAM devices performing the memory read operation;

the logic in response to the third module control signals enables the second set of tristate buffers for a third time period corresponding to the subsequent memory read operation to drive a respective n-bit section of the additional read data; and

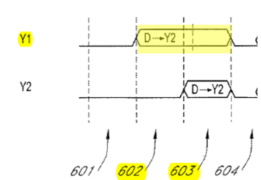
the logic is further configurable to disable the second set of tristate buffers after the second time period and before the third time period.</td></tr>
<tr><td>[34]</td><td>The memory module of claim 27, wherein the first set of tristate buffers are enabled for the first time period in accordance with a latency parameter.</td></tr>
<tr><td>[35]</td><td>The memory module of claim 27, wherein the second set of tristate buffers are enabled for the second time period in accordance with a latency parameter.</td></tr>
</table>

I. The Board Previously Found Similar "Latency" Limitations Obvious (POPR 16–20, 28–51)

Claim limitation [1.e] is obvious, *see* Pet. at 73–81, and not patentably distinct from claims 8, 20, 25, and 31 of the parent 907 Patent, *see* POPR at 18, which the Board found obvious in light of Ellsberry, EX1062 at 62–63. The prior invalidation of claims 8, 20, 25, and 31 compels a finding that [1.e] is obvious, based both on the Board's reasoning, *see id.*, and collateral estoppel, Pet. at 42–44.

All of those claims, like [1.e], require the transmission of data through the buffer to be done "in accordance with a ***latency*** parameter." The 339 Patent admits "latency" was known in the prior art: "***As is known***, Column Address Strobe (CAS) latency is a delay time…." EX1001 at 15:61–:66. Indeed, CAS latency was standardized by JEDEC and measured in clock cycles (e.g., 3 or 4). Pet. at 36–37, 75–77; EX1009 at 9–10; EX1011 at 11–12, 22; EX1051 at 12–14, 24–25.

The 339 Patent does not disclose any details of how "latency" should be taken into account, conceding it would be obvious. EX1001 at 15:66–16:7. For example, Figure 6 just shows generic time periods (e.g., 602, 603, etc.), and the description provided in the specification (*id.* at 18:5–:24) conflicts with what is shown in Figure 6 (to the right), leaving it to the POSITA to figure out. In short, "the [asserted] patent itself does not



disclose the level of detail that [the patent owner] would have us require of the prior art." *Lockwood v. Am. Airlines, Inc.*, 107 F.3d 1565, 1570 (Fed. Cir. 1997).

Netlist argues [1.e] is nonobvious over Ellsberry+Halbert (ignoring the prior invalidity ruling based on Ellsberry) because "Halbert's write path is ***enabled*** for a time period ***far longer*** than the period during which data is being actively driven." POPR at 30, 34–35, 49–51. But that is not what Halbert's figure shows, Pet. at 79–80, because Halbert's DIR signal ***alone*** does not enable the data path to drive the data, EX1006 at 7:3–:4 (WRITE state entered "[u]pon sensing the first WRITE command"). Given that data lines are bi-directional, they would not be enabled in one direction (e.g., write) longer than necessary, because that would create a conflict with data in the other direction (e.g., read). Pet. at 31–32, 45–47, 78, 81.

Furthermore, Netlist's attack on Halbert is precluded by another Final Written Decision by the Board, this time involving U.S. Patent No. 8,756,364 (EX1081), which is part of the family of prior-art patents filed in 2005 incorporated by reference in the 339 Patent. EX1001 at 10:50–:53; EX1003, ¶¶53–58; Pet. at 20–26. The Board found that Halbert (EX1082/EX1006), in light of the known CAS latency, renders obvious "wherein the first logic element controls the second logic element to selectively ***enable*** the data communication according to the ***latency*** value," EX1080 at 3, 7–12, directly contrary to Netlist's argument here.

Netlist also argues that the "latency" must affect the ***duration*** of the "first time period" (as opposed to just the ***start*** of that time period). POPR at 35–37. But nothing in the patent or the claims requires the latency to affect the duration:

the "latency parameter," as the patent explains, "is known" as "a delay time" which indicates "the ***moment*** the data…is on the output pins." EX1001 at 15:61–16:6. The "latency" determines the start, not the duration, of the data transfer. EX1009 at 10 ("delay, in clock cycles, between…command and…***first*** piece of output data"); Pet. at 75–77; EX1011 at 22; EX1051 at 24–25.

Netlist argues "Ellsberry does not involve enabling or disabling data paths," POPR at 37–43, but the Board rejected that argument in the 907 Final Written Decision, which found that Ellsberry teaches enabling a data path through one port (e.g., Port A) while disabling the data path through the other port (e.g., Port B) — which Netlist itself referred to as the "one-port disabled" embodiment. Pet. at 149–51; EX1062 at 15–16, 19–21, 31–37.

Netlist argues incorporating Halbert's "tristate buffers" into Ellsberry would have been "redundant" given that Ellsberry already teaches a "single load," POPR at 43–45, but Ellsberry's Figure 4 is not the "single load" implementation, which is why a POSITA would have been motivated to add "tristate buffers" as taught by Halbert to create the "single load" disclosed by Ellsberry, Pet. at 33–35, 44–47.

II. The Examiner Properly Found The "Latency" Limitations Obvious, But Erred By Ignoring the Board's Final Written Decision (POPR 69–83)

During prosecution, the Examiner correctly rejected [1.e] as obvious in light of the JEDEC standards, EX1002 at 692–93, and the Examiner told Netlist that "an[] amendment [to the claim] would be required" to distinguish this limitation

from the prior art, POPR at 71 (quoting EX1002 at 813). But after this rejection, Netlist did ***not*** substantively amend [1.e]:

> wherein the each respective byte-wise buffer further includes logic configurable to control the byte-wise data path in response to the module control signals, wherein ~~the logic is configurable to enable~~ the byte-wise data path is enabled for a ~~specific~~ first time period in accordance with a latency parameter to actively drive a respective byte-wise section of the N-bit wide write data associated with the memory operation from the first side to the second side during the first ~~specific~~ time period ~~in response to the module control signals~~; and

Pet. at 42. Netlist changed "configurable to enable" to "is enabled," and changed "specific time period" to "first time period," but the "time period" ***remained*** the time needed to "drive…[the] data associated with the memory operation," and the limitation "in accordance with a latency parameter" did ***not*** change. As a result, [1.e] is still obvious in light of the JEDEC standards, *see* Pet. at 75–81, contrary to Netlist's arguments, POPR at 69–76.

With respect to [1.f], however, which was amended to require "tristate buffers," Pet. at 42, the Examiner materially erred by (1) ignoring the Board's finding that it would be obvious to use tristate buffers in Figure 4 of Ellsberry, Pet. at 33; EX1062 at 69–71, 74–75; (2) ignoring the Board's rejection of Netlist's arguments about "no-ports disabled," Pet. at 148–52, which Netlist still persists in repeating, POPR at 77–83; and (3) not considering the combination of Ellsberry and Halbert, which clearly renders [1.f] obvious, Pet. at 146–48, 81–86, 44–47.

Dated: August 26, 2022

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CERTIFICATE OF COMPLIANCE

I hereby certify that this Petitioner's Authorized Reply to Patent Owner's Preliminary Response, excluding the parts of the brief exempted by 37 C.F.R. § 42.24, complies with the page limits provided by the Board in Paper No. 10 (Aug. 22, 2022), which stated: "Any preliminary reply filed by Petitioner will be limited to 4 pages and will be due to be filed by August 26, 2022."

Dated: August 26, 2022

Respectfully submitted,

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that on this 26th day of August, 2022, **Petitioner's Authorized Reply to Patent Owner's Preliminary Response** was served by email on the following counsel for Patent Owner:

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